Customer No.: 31561
Application No.: 10/707,668
Docket NO.: 09133-US-PA-/

AMENDMENTS

Please amend the application as indicated hereafter.

In the Title:

Please change the title of the invention to "FABRICATION METHOD OF A FLASH MEMORY DEVICE".

In the Specification:

Please replace paragraph [0008] with the following amended paragraph:

[0008] Referring to Figure 1, Figure 1 is a schematic diagram, illustrating the structure of a conventional stacked gate flash memory (US patent 6214668). A conventional flash memory device is formed with a p-type substrate 100, a deep N-type well region 102, a P-type well region 104, a stacked gate structure 106, a source region 108, a drain region 110, a spacer 112, an inter-layer dielectric layer 114, a contact 116 and a conductive line 118. The stacked gate structure 106 comprises a tunnel oxide layer 120, a floating gate 122, a gate dielectric layer 124, a control gate 126 and a gate cap layer 128. The deep N-type well 102 is located in the P-type substrate 100. The stacked gate structure 106 is disposed on the substrate 100. The source region 108 and the drain region 110 are located beside the sides of the stacked gate structure 106 in the P- type substrate 100. The spacer 112 is disposed on the sidewall of the stacked gate structure 106. The P-type well region 104 is located in the N-type deep well region 102, extending from the drain region 110 to substrate 100 underneath the stacked gate structure 106. The interlayer dielectric layer 114 is disposed on the P-type substrate 100. The contact 116 penetrates through the inter-layer dielectric layer 114 and the substrate 100, short-circuiting the P-type well region 104 and the drain region 110. The conductive line 118 is disposed above the interlayer dielectric layer 114 and electrically connected with the contact 116.

Please replace paragraph [0009] with the following amended paragraph:

[0009] During the fabrication of the flash memory device illustrated in Figure 1, the P-type well region 104 is formed by forming a mask layer (not shown) on the entire P-type substrate 100 subsequent to the formation of the stacked gate structure 106. This mask layer exposes a pre-determined region for forming the drain region. A tilt angle (0 degrees to 180 degrees) ion implantation process is then conducted to implant dopants to the deep N-type well region 102 in the P-type substrate 100 near the drain region on one side of the stacked gate structure 100, using the stacked gate structure 106 and the mask layer as a mask. A drive-in process is then performed to extend the P-type well region 104 to the substrate 100 under the stacked gate structure 106.

Please replace paragraph [0031] with the following amended paragraph:

[0031] The P-type substrate 200 comprises a trench 234. The deep N-type well region 202 is located in the P-type substrate. The spacer 212a and the spacer 212b are disposed on the sidewall of the stacked gate structure 206, wherein the spacer 212a is directly connected to the top of the trench 234. The source region 208 is located in the P-type substrate 200 under the spacer 212a, while the drain region is located in the P-type substrate 200 under the spacer 212b. A P-type well is located between the deep N-type well region ~~202~~ 202 and the stacked gate structure 206, wherein the junction between the P-type well region 204 and the deep N-type well region 202 is higher than the bottom of the trench 234. A doped region is located on the sidewall and the bottom of the trench 234. The doped region 209 is connected to the source region 208, wherein the doped region isolates

the p-type well region from the subsequently formed contact 216. The contact 214 penetrates the junction between the drain region 210 and the p-type well region 204, short-circuiting the drain region 210 and the p-type well region 204. The contact 216 fills the trench in the p-type substrate and electrically connects with the source region 208. The interlayer dielectric layer 218 is disposed above the P-type substrate 200. A plug 220 is disposed in the interlayer dielectric layer 218, electrically connecting to the contact 214. A conductive line 222 is disposed on the interlayer dielectric layer 218, electrically connecting to the plug 220.

Please replace paragraph [0032] with the following amended paragraph:

[0032] According to the above embodiment of the present invention, the source region 208 is located in the substrate 200 under the spacer 212a and is connected to the doped region 209 at the sidewall and the bottom of the trench 234. This doped region 209 can prevent an electrical short between the subsequently formed contact 216 and the p-well region ~~240~~204. Further the contact 216 (tungsten source line) connects the source region 208 of each memory cell to lower the resistance of the source line without the formation of a source line pickup in the active region. The integration of the device is also increased.

Please replace paragraph [0044] with the following amended paragraph:

[0044] Referring to Figure 3F, a patterned photoresist layer 328 is formed on the entire substrate 300. This patterned photoresist layer 328 exposes the source region 320.

An etching is then conducted using the patterned mask layer 328 and the stacked gate structure 318 as a mask, wherein the substrate 300 is etched into the N-type well region 304 to form a trench 330 and a source region 320a, wherein the source region 320a is located under the spacer 324. The bottom of the trench 330 and the sidewall of the trench 330 form an obtuse angle θ. Further, the trench 300 segments the P-type well region 306 to form the P-type well region 306a, wherein this P-type well region 306a is formed between the source regions 320a of two neighboring memory cells. An ion implantation process is then conducted to implant dopants to the substrate 300 along the sidewall and the bottom of the trench 330 to form a doped region 332, using the stacked gate structure 318 and the patterned photoresist layer 328 as a mask. The implanted dopants include, for example, N-type dopants, such as, arsenic ions or phosphorous ions. If the implanted dopants are arsenic ions, the implantation energy is about 60000 volts and the implanted dosage is about $1x10^{15}$ atoms/cm^2. If the implanted dopants arephosphorous ions, the implantation energy is about 30000 volts and the implanted dosage is about $1x10^{15}$ atoms/cm^2. The dopants are implanted with a method includes the tilt angle implantation at a tilt angle of, for example, 15 degrees to 30 degrees. The doped region 332 can isolate the subsequently formed contact from the P-type well region 306a to prevent a short-circuit between the contact and the P-type well region 306a. Thereafter, the patterned photoresist layer 328 is removed. Referring to Figure 3G, a contact 336 (source line) is formed above the source region 320a between the gate structures 318 and a contact 338 is formed on the P-type well region 306a between the gate structures 318. The contact (source line) 336 and the contact

338 are formed with, for example, tungsten. The contact 336 (source line) and the contact 338 are formed by, for example, forming a conductive layer (not shown) on the substrate 300 and this conductive layer fills the space between the gate structures 318. A chemical mechanical polishing or back-etching process is then performed until the cap layer 316 of the gate is exposed to form the contact 336 (source line) on the source region 320s between the gate structures 318 and the conductive layer(not shown) on the P-type well region 306a between the gate structures 318. The conductive layer (not shown) is, for example, a strip of conductive layer, approximately parallel to the contact 336. A photolithography and etching are performed to remove a portion of the conductive layer to form an opening in the conductive layer (not shown). This opening isolates the contact 338 of neighboring memory cells. The contact 338 penetrates to the junction between the drain region 322a and the P-type well region 306 to electrically short-circuit the drain region 322a and the P-type well region 306.